We claim:

1. A method for forming a semiconductor device comprising the steps:

providing a substrate including a support region and an array region having an array device diffusion region;

depositing a dielectric layer on said substrate;

forming a patterned hardmask on said dielectric layer, said patterned hardmask having a first opening that overlays at least a portion of said array device diffusion region;

partially etching said dielectric layer selective to said hardmask through said first opening to form a first recess in said dielectric layer;

forming a second mask having a second opening at least partially overlapping a portion of said first recess; and

subsequently etching said dielectric layer selective to said hardmask through said second opening and through said portion of said first recess,

so that said portion of said first recess is extended through said dielectric layer to form a second recess so that a corresponding portion of said array device diffusion region is exposed.

2. The method of claim 1, further comprising, after said step of subsequently etching:

removing said second mask;

forming a first conductive feature in said second recess; and

forming a second conductive feature in said first recess.

3. The method of claim 1 wherein said second mask further comprises a block mask over said support region.

4. The method of claim 2 wherein said first conductive feature comprises a contact structure and said second conductive feature comprises an interconnect structure.

5. The method of claim 1 wherein said second opening defines a contact via.

6. The method of claim 1 wherein said patterned hardmask defines an interconnect feature, and said second mask comprises a line-type opening that is oriented to intersect said interconnect feature at an angle.

7. The method of claim 6 wherein said angle is approximately 90 degrees.

8. The method of claim 1 wherein said second mask is completely open in said array region.

9. The method of claim 3 wherein said second mask is completely open in said array region.

10. The method of claim 1 wherein said array region further comprises a memory device corresponding to said array device diffusion region.

11. The method of claim 10 wherein said memory device comprises a gate stack including an encapsulating dielectric positioned adjacent to said array device diffusion region, and wherein said method further comprises filling said second recess with a conductive material to form a borderless contact.

12. The method of claim 10 wherein said memory device further

comprises a vertical transistor.

13. The method of claim 1 wherein said support region includes a support device diffusion region, wherein said patterned hardmask includes a third opening that overlays at least a portion of said support device diffusion region and

said step of partially etching further comprises simultaneously etching through said third opening to form a third recess, and

wherein said second mask further comprises a fourth opening at least partially overlapping a portion of said third recess and

said step of subsequently etching further comprises simultaneously etching through said fourth opening and through said portion of said third recess

so that said portion of said third recess is extended through said dielectric layer to form a fourth recess so that a corresponding portion of said support device diffusion region is exposed.

14. The method of claim 13, further comprising, after said step of subsequently etching:

removing said second mask;

depositing a conductive material in said second recess and said fourth recess to form contact structures; and

depositing a second conductive material in said first recess and said third recess to form interconnect structures.

15. A semiconductor device comprising:

a substrate including device diffusion region;

a dielectric layer on said substrate;

a contact structure formed in said dielectric layer; and

an interconnect structure formed in said dielectric layer over

said contact structure,

so that said contact structure is in contact with said device diffusion region and said interconnect structure and wherein said contact structure and said interconnect structure are aligned with each other.

16. The semiconductor device of claim 15, wherein said contact structure comprises a first conductive material and said interconnect structure comprises a second conductive material.

17. The semiconductor device of claim 16, wherein said first conductive material and said second conductive material consist essentially of the same conductive material.

18. The semiconductor device of claim 15, wherein said substrate further comprises an array region including a vertical memory device comprising said device diffusion region.

19. The semiconductor device of claim 15, wherein said substrate further comprises a gate stack including an encapsulating material adjacent to said device diffusion region wherein said contact structure and said encapsulating material share a boundary.

20. The semiconductor device of claim 15, wherein said substrate further comprises an array region and a support region,

said array region including an array device diffusion region and an array interconnect structure and

said support region including a support device diffusion region and a support interconnect structure, and

further comprising an array contact structure in contact with said array device diffusion region and said array interconnect structure and

further comprising a support contact structure in contact with said support device diffusion region and said support interconnect structure,

wherein said array contact structure is aligned with said array interconnect structure and said support contact structure is aligned with said support interconnect structure.